

REMARKS

Favorable reconsideration of this application in view of the remarks to follow and allowance of the claims of the present application are respectfully requested.

Before addressing the merits of the rejections in the present Office Action, applicants have amended Claim 1 to further define the location of the underlying oxide region. More specifically, applicants have inserted the terms "in the SOI layer and" between the phrases "the presence of an underlying localized oxide region that is located" and "on top of and in contact with". This amendment can find support in paragraphs [0064] and [0065] of the specification, and FIGS. 5 and 7-10. of the specification as well. Applicants have also amended Claim 1 to positively define that the localized oxide region has outer edges that are aligned to outer edges of the gate region. Support for this amendment is seen in FIG. 10 of the present application, for example. Claim 15 has been amended in a similar fashion to Claim 1.

Since the above amendments do not introduce any new matter into the present application, entry thereof is respectfully requested.

Claims 1, 2, 6, 9, 10, and 15 stand rejected under 35 U.S.C. §102(b) as allegedly anticipated by or, in the alternative, under 35 U.S.C. §103(a) as allegedly obvious over the disclosure of U.S. Patent 6,064,092 to Park, et al. (hereinafter "Park et al."). Further, Claims 3, 7, and 14 stand rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Park et al.

Applicants respectfully submit that Claim 1, as amended, is not anticipated by the disclosure of Park et al. since the applied reference does not teach the claimed semiconducting device recited in Claim 1. That is, Park et al. do not disclose a semiconducting device comprising a channel region located in an SOI layer of an SOI substrate, wherein said channel region is thinned by the presence of an underlying localized oxide region that is located in the

SOI layer and on top of and in contact with a buried insulating layer of said SOI substrate, said localized oxide region has outer edges that are aligned to outer edges of a gate region that is located above said channel region.

It is axiomatic that anticipation under §102 requires that the prior art reference disclose each and every element of the claim to which it is applied. *In re King*, 801 F.2d, 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1996). Thus, there must be no differences between the subject matter of the claim and the disclosure of the prior art reference. Stated another way, the reference must contain within its four corners adequate direction to practice the invention as claimed. The corollary of the rule is equally applicable: Absence from the applied reference of any claimed element negates anticipation. *Kloster Speedsteel AB v. Crucible Inc.*, 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

Park et al. disclose a semiconductor-on-insulator substrate comprising an insulating layer 60 having a surface thereon and a trench therein; a semiconductor region 73; and a mesa insulating region 60a on the bottom of the trench, wherein said semiconductor region 73 is thinned by said mesa insulating region 60a. Notably, the mesa insulating region 60a is in the insulating layer 60. Park et al. specifically teach that the insulating layer 60 contains the mesa insulating region 60a (column 3, lines 63-66). Further, Park et al. teach that the mesa insulating region 60a is formed by polishing down the semiconductor substrate 40 to a semiconductor region 40' while the insulating layer 60 is bonded directly to a handling substrate 100 (See FIG. 3D, FIG. 3E, lines 53 to 67 of column 3, and lines 1-6 of column 4). Thus, the mesa insulating region 60a is not a different layer, but an integral part of the insulating layer 60. That is, the mesa insulating region 60a is merely a flat-topped elevation of the insulating layer 60. In contrast, the underlying localized oxide region 25 of the present invention is in a different layer

14, i.e., the SOI layer, and is located on top of and in contact with the buried insulating layer 13 (See FIGS. 5 and 7-10, and paragraphs [0064] and [0065]). Therefore, the semiconductor-on-insulator substrate of Park et al. is structurally different from the semiconducting device of the present invention. Since Claims 2, 6, 9, 10, and 15 are dependent on Claim 1 and include all the limitations thereof, Park et al. do not disclose the subject matter of Claims 2, 6, 9, 10, and 15 either.

In addition, applicants respectfully submit that Claim 1 now positively recites that the localized oxide region in the SOI layer has outer edges that are aligned with outer edges of the overlying gate region, while Park et al. shows that region 60a has outer edges not aligned with the outer edges of the gate region. As such, applicants submit that the claimed structure is not anticipated by the disclosure of Park et al. Applicants observe that the same basic arguments are applicable to Claim 15 as well.

In view of the above, Park et al. fail to disclose each and every element of the claims to which it is applied, and thereby do not anticipate the present invention. The rejection under 35 U.S.C. §102(b) has been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

With respect to the §103(a) rejections, applicants respectfully submit that the Examiner fails to establish a *prima facie* case of obviousness as discussed below.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the reference itself or in the knowledge generally available to one of ordinary skill in the art, to modify the reference. Second, there must be a reasonable expectation of success. Finally, the cited reference must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed

combination and the reasonable expectation of success must both be found in the reference, not based on applicants' disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

First, Park et al. neither disclose nor remotely suggest a semiconducting device comprising the same physical structure of the semiconducting device of the present invention.

Second, there is no suggestion available in Park et al. which motivates one skilled in the art to modify the disclosed mesa insulating region 60a, which is part of the insulating layer 60, in such a way to arrive at the presently claimed underlying localized oxide region 25, which is in a different layer 14. In fact, the methods of forming the mesa insulating region 60a of Park et al. are drastically different from those of forming the underlying localized oxide region 25 of the present invention. The mesa insulating region 60a is formed by polishing down the semiconductor substrate 40 to a semiconductor region 40' while the insulating layer 60 is bonded directly to a handling substrate 100 (lines 53 to 67 of column 3, and lines 1-6 of column 4). In contrast, the underlying localized oxide region 25 of the present invention is formed by conducting an oxygen implantation 40 at a certain implant energy, implant dose, and dummy gate region height. Applicants further observe that region 60a of Park et al. does not have outer edges that are aligned to outer edges of the gate region. Therefore, applicants respectfully submit that one skilled in the art, in view of the physical structure of the semiconductor-on-insulator substrate of Park et al. and the methods of forming the same, would not readily envision a structurally different semiconducting device that is formed through different methods, such as the semiconducting device of the present invention.

In view of the above, applicants respectfully submit that Park et al. do not render the present invention obvious. The rejections under 35 U.S.C. §103(a) have been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

Claims 4, 5, 8, and 10-13 stand rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Park et al. further in view of the disclosure of U.S. Patent No. 6,479,866 to Xiang (hereinafter "Xiang"). Claim 6 stands rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Park et al. further in view of the admitted prior art. More specifically, the Examiner alleges that Xiang teaches that the damaged region 90 can be formed separately from the buried insulating layer 20.

Applicants respectfully submit that the present invention is not rendered obvious by Park et al. further in view of Xiang because there is no suggestion available in the cited references which motivates one skilled in the art to modify the disclosed devices in such a way to arrive at the device of the present invention.

As discussed previously, Park et al. not only fail to teach or recognize applicants' claimed semiconducting device in which the channel region is thinned by the presence of an underlying localized oxide region that is in the SOI layer, but also fail to provide any suggestion which motivates one skilled in the art to form the mesa region 60a in the SOI layer. Park et al. also do not teach or suggest a structure in which region 60a has outer edges that are aligned to outer edges of an overlying gate region. Xiang discloses a semiconductor-on-silicon device having reduced floating body effects. More specifically, Xiang intends to resolve the problem of undesirable floating body effects in field effect transistors (column 3, line 62 to column 4, line 10), and provides a transistor having one or more damaged recombination regions within the body of the transistor. In contrast, the present invention intends to resolve the problem of high external resistance in ultra-thin channel SOI devices, and provides a thin SOI device having low external resistance without raised source/drain regions. Notably, Xiang does not in any manner comment on the problem of high external resistance in ultra-thin channel SOI devices. With

regard to the damaged region 90, Xiang specifically teaches that the presence of the damaged region 90 within the body 38 greatly increases the recombination rate within the body, thus reduces the tendency of the body to build up a floating body potential (column 4, lines 3-10). Xiang also teaches the location and size of the damaged region 90. However, Xiang does not suggest applying the damaged region 90 to a semiconducting device of Park et al. in such a way to form the mesa region 60a of Park et al. in the SOI layer. Thus, there is no motivation provided in the applied references, or otherwise of record, to modify the disclosed semiconductor-on-insulator substrates to include applicants' claimed semiconducting device. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." *In re Vaeck*, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

The various §103 rejections also fail because one skilled in the art, in view of the cited references, would not have a reasonable expectation of success to employ the damaged region 90 of Xiang, which is taught to reduce floating body effects, into the semiconducting device of Park et al. for the purpose of reducing the high external resistance of ultra thin SOI devices.

The rejections under 35 U.S.C. §103 have been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

This in view of the foregoing amendments and remark it is firmly believed that

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